N-Ch + P-Ch Fast Switching MOSFET

•General Description

The LH4012 uses trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.This device is suitable for high current load applications.

BVDSS	$RDS_{(0N)}$	ID
40	19	30
-40	34	-20

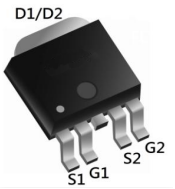
■ RoHS COMPLIANT

•Features

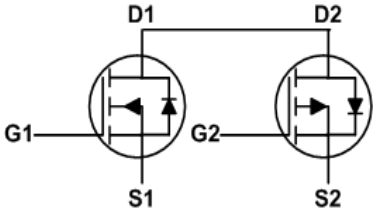
■Advance high cell density trench technology
■Low RDS(ON) to minimize conductive loss
■Low Gate Charge for fast switching

•Application

■Lighting
■Power Supplies



TO-252-4



•Ordering Information:

Part Number	LH4012
Package	TO-252-4
Basic Ordering Unit (pcs)	2500
Normal Package Material Ordering Code	LH4012T7-TO252-4-TAP
Halogen Free Ordering Code	LH4012T7-TO252-4-TAP-HF

•Absolute Maximum Ratings（TC =25℃）

PARAMETER	SYMBOL	Value		UNIT
		N-Ch	P-Ch	
Drain-Source Breakdown Voltage	BV_{DSS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current ,T_C = 25°C[1]	I_D	30	-20	A
Continuous Drain Current ,T_C = 100°C[1]	I_D	18	-16	A
Pulsed drain current (TC = 25°C, tp limited by Tjmax)[2]	I_{DM}	46	-40	A
Single Pulse Avalanche Energy[3]	E_{AS}	28	66	mJ
Power Dissipation[4]	$P_D(T_C$=25℃)	25	31.3	W
Operating Temperature	T_J	-55~+150	-55~+150	℃
Storage Temperature	T_{STG}	-55~+150	-55~+150	℃

●N-Channel Electronic Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D=250uA	40	--	--	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25℃,I_D=1mA	--	0.034	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	1.0	1.5	2.5	V
$V_{GS(TH)}$ Temperature Coefficient	$\Delta V_{GS(TH)}$		--	-4.56	--	V
Drain-source On Resistance[2]	$R_{DS(ON)}$	V_{GS} =10V, I_D=12A	--	19	25	mΩ
		V_{GS} =4.5V, I_D=10A	--	24	35	
Drain-Source Leakage Current	I_{DSS}	V_{DS}=32V,V_{GS}=0V,T_J=25℃	--	--	1	uA
		V_{DS}=32V,V_{GS}=0V,T_J=55℃	--	--	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20,V_{DS}=0V	--	--	±100	nA
Forward Transconductance	G_{FS}	V_{DS} =5V, I_D=12A	--	8	--	S
Gate Resistance	Rg	V_{DS}=0V,V_{GS}=0V,f=1MHz	--	2.6	5.2	Ω
Input Capacitance	Ciss	V_{GS}=0V, V_{DS}=15V, f=1.0MHz	--	593	--	pF
Output Capacitance	Coss		--	76	--	
Reverse transfer Capacitance	Crss		--	56	--	
Turn-On Delay Time	$Td_{(on)}$	V_{DD}=20V, V_{GS}=10V, R_G=3.3Ω, I_D=1A	--	8.9	--	nS
Turn-Off Delay Time	$Td_{(off)}$		--	41	--	
Turn-On Rise Time	T_r		--	2.2	--	
Turn-Off Fall Time	T_f		--	2.7	--	
Total Gate Charge	Qg	I_D=12A, V_{DS}=20V, V_{GS}=4.5V	--	5.5	---	nC
Gate-to-Source Charge	Qgs		--	1.25	--	
Gate-to-Drain Charge	Qgd		--	2.5	---	
Continuous Diode Forward Current[1,5]	I_S	V_{Gs}=V_{DS}=0V, Force Current	--	--	23	A
Pulsed Diode Forward Current[2,5]	I_{SM}		--	--	46	A
Diode Forward Voltage[2]	V_{SD}	Tj=25°C, Is=-20A, V_{GS} =0V	--	--	1.2	V

Notes:

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper;

2.The data tested by Pulsed,Pulse width ≤ 300μs, Duty cycle ≤ 2%;

3.The EAS data shows Max. rating.The Test condition is L=0.1mH,I_{AS}=17.8A,V_{DD}=25V,V_{GS}=10V;

4.The Power Dissipation is limited by 150℃ junction temperature;

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

●P-Channel Typical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250uA	-40	--	--	V
BVDSS Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25℃,I_D=-1mA	--	0.012	--	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0	-1.5	-2.5	V
$V_{GS(TH)}$ Temperature Coefficient	$\Delta V_{GS(TH)}$		--	-4.32	--	V
Drain-source On Resistance[2]	$R_{DS(ON)}$	V_{GS} =-10V, I_D=-8A	--	34	40	mΩ
		V_{GS} =-4.5V, I_D=-5A	--	47	65	
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-32V,V_{GS}=0V,T_J=25℃	--	--	1	uA
		V_{DS}=-32V,V_{GS}=0V,T_J=55℃	--	--	5	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20,V_{DS}=0V	--	--	±100	nA
Forward Transconductance	G_{FS}	V_{DS} =-5V, I_D=-8A	--	12.6	--	S
Gate Resistance	Rg	V_{DS}=0V,V_{GS}=0V,f=1MHz	--	13	16	Ω
Input Capacitance	Ciss	V_{GS}=0V, V_{DS}=-15V, f=1.0MHz	--	1004	--	pF
Output Capacitance	Coss		--	108	--	
Reverse transfer Capacitance	Crss		--	80	--	
Turn-On Delay Time	$Td_{(on)}$	V_{DD}=-15V, V_{GS}=-10V, R_G=3.3Ω, I_D=1A	--	19.2	--	nS
Turn-Off Delay Time	$Td_{(off)}$		--	48.6	--	
Turn-On Rise Time	T_r		--	12.8	--	
Turn-Off Fall Time	T_f		--	4.6	--	
Total Gate Charge	Qg	I_D=-12A, V_{DS}=-20V, V_{GS}=-4.5V	--	9	---	nC
Gate-to-Source Charge	Qgs		--	2.54	--	
Gate-to-Drain Charge	Qgd		--	3.1	---	
Continuous Diode Forward Current[1,5]	I_S	V_{Gs}=V_{DS}=0V, Force Current	--	--	-20	A
Pulsed Diode Forward Current[2,5]	I_{SM}		--	--	-40	A
Diode Forward Voltage[2]	V_{SD}	Tj=25°C, Is=-1A, V_{GS} =0V	--	--	-1.2	V

●Thermal Characteristics

PARAMETER	SYMBOL	MAX	UNIT
Thermal Resistance Junction-case[1]	Rth_{JC}	5	℃/W
Thermal Resistance Junction-ambient[1]	Rth_{JA}	62	℃/W

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper;

2.The data tested by Pulsed,Pulse width ≤ 300μs, Duty cycle ≤ 2%;

3.The EAS data shows Max. rating.The Test condition is L=0.1mH,I_{AS}=-20A,V_{DD}=-25V,V_{GS}=-10V;

4.The Power Dissipation is limited by 150℃ junction temperature;

5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

●N-Ch Typical Characteristics

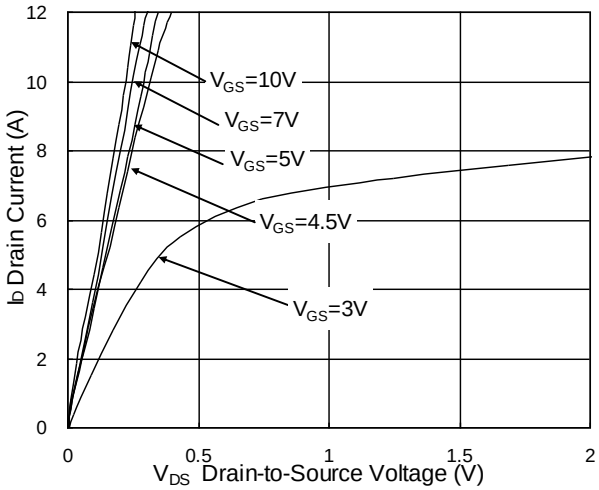


Fig.1 Typical Output Characteristics

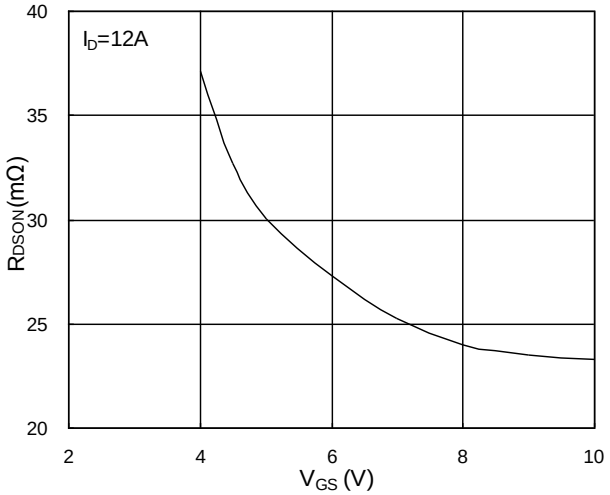


Fig.2 On-Resistance vs. G-S Voltage

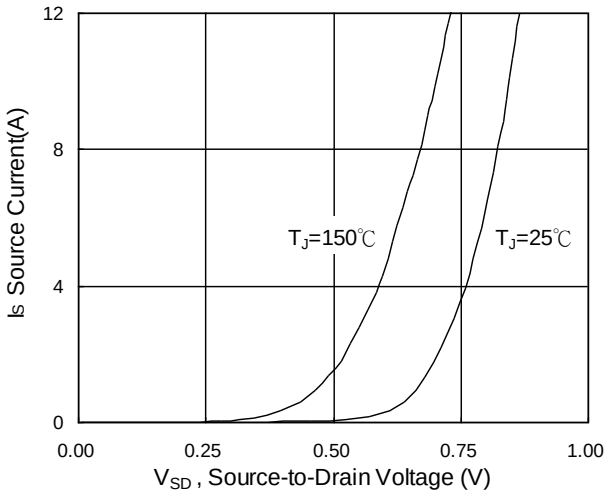


Fig.3 Forward Characteristics of Reverse

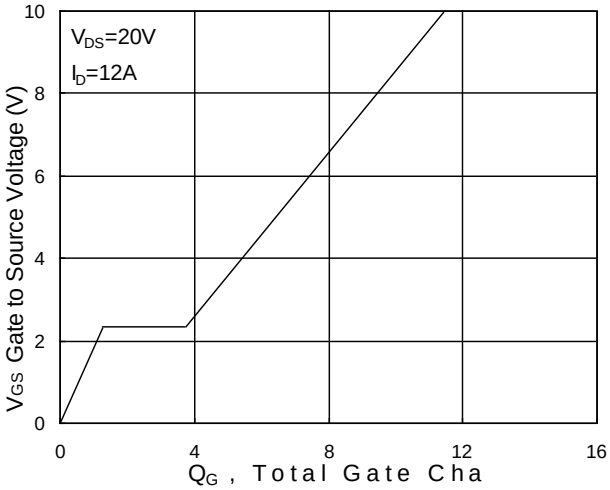


Fig.4 Gate-Charge Characteristics

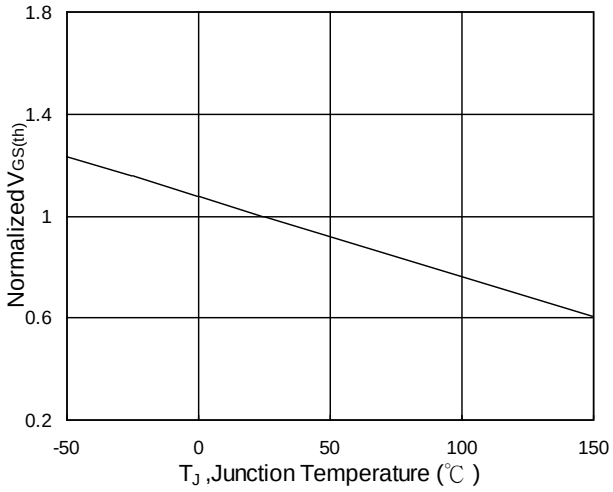


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

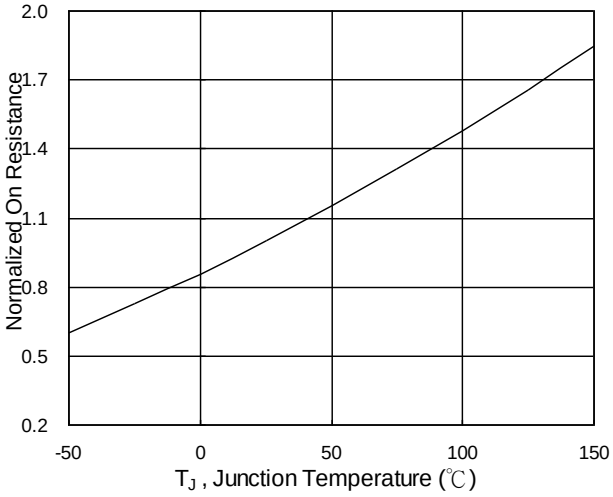


Fig.6 Normalized R_{DSON} vs. T_J

●N-Ch Typical Characteristics(Cont.)

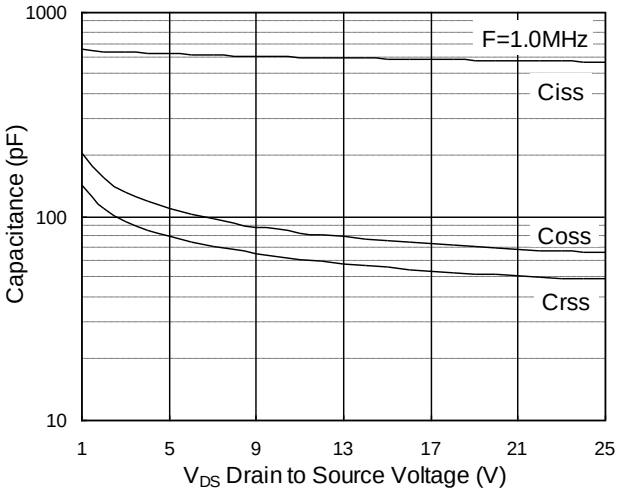


Fig.7 Capacitance

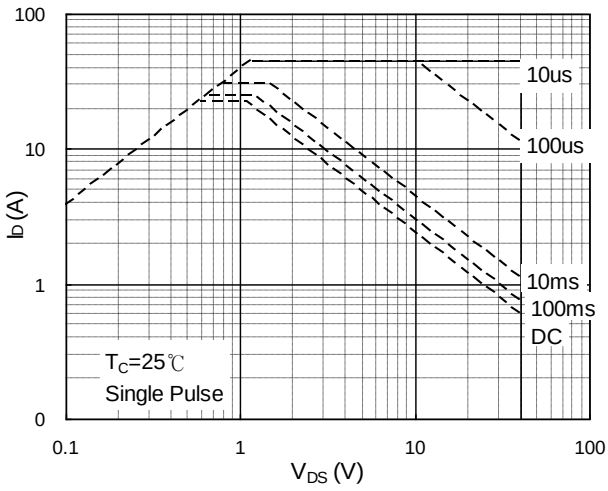


Fig.8 Safe Operating Area

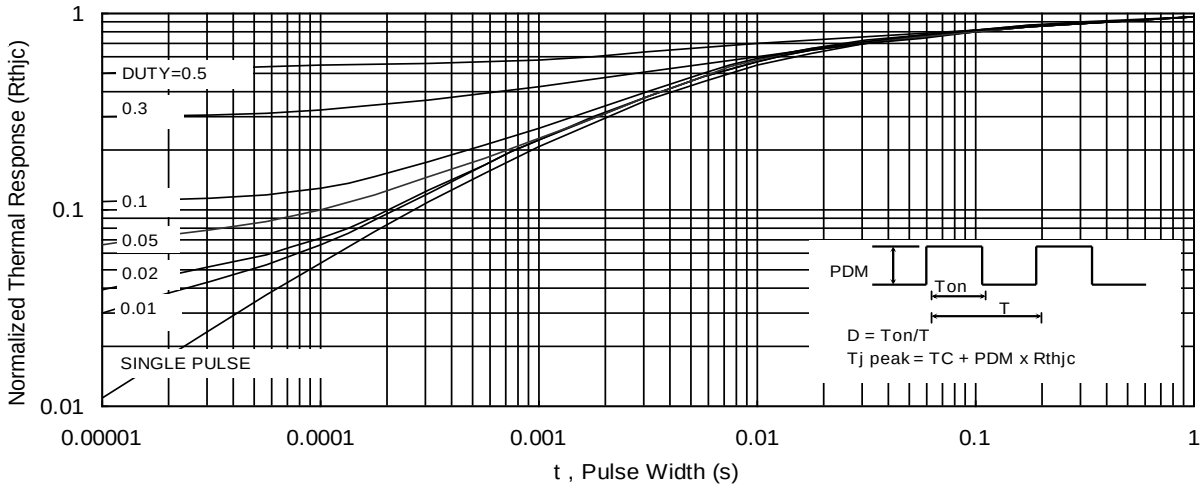


Fig.9 Normalized Maximum Transient Thermal Impedance

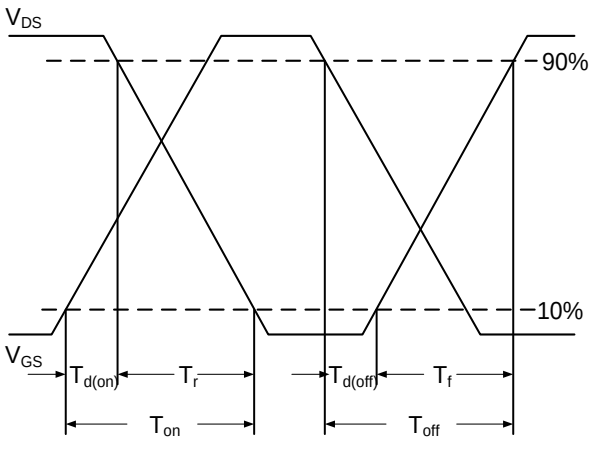


Fig.10 Switching Time Waveform

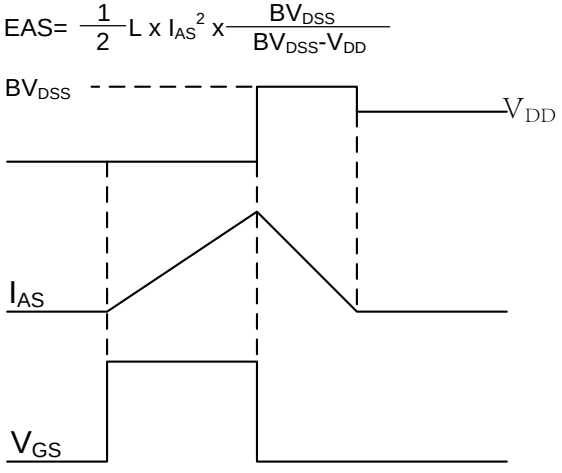


Fig.11 Unclamped Inductive Switching Wave

● P-Channel Typical Characteristics

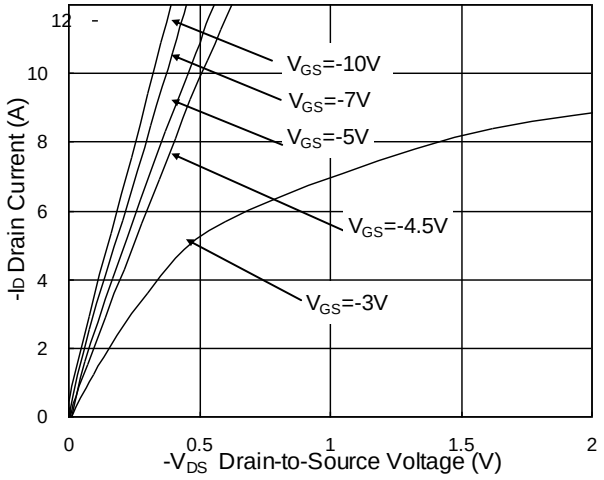


Fig.1 Typical Output Characteristics

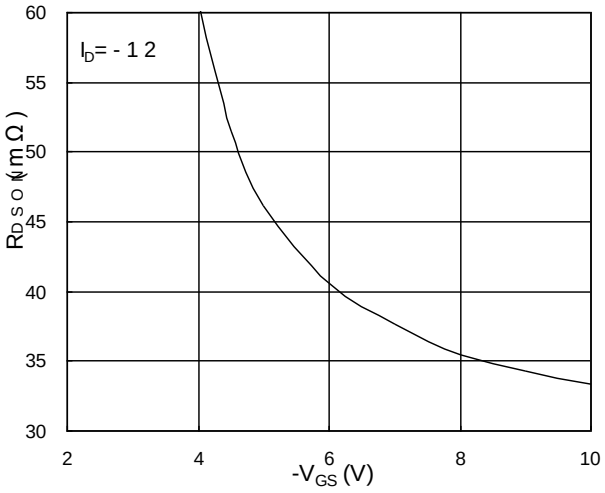


Fig.2 On-Resistance v.s Gate-Source

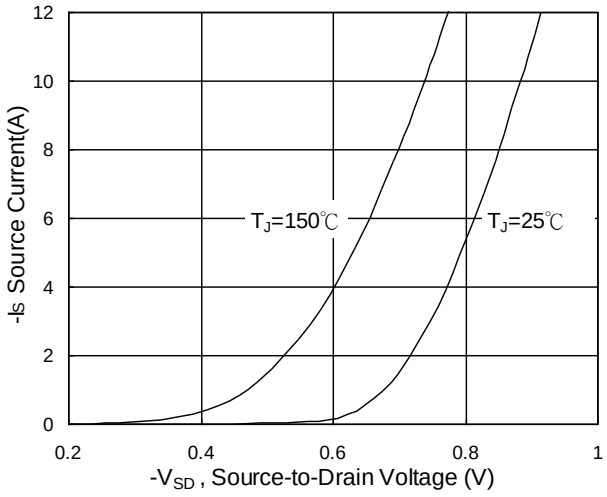


Fig.3 Forward Characteristics of Reverse

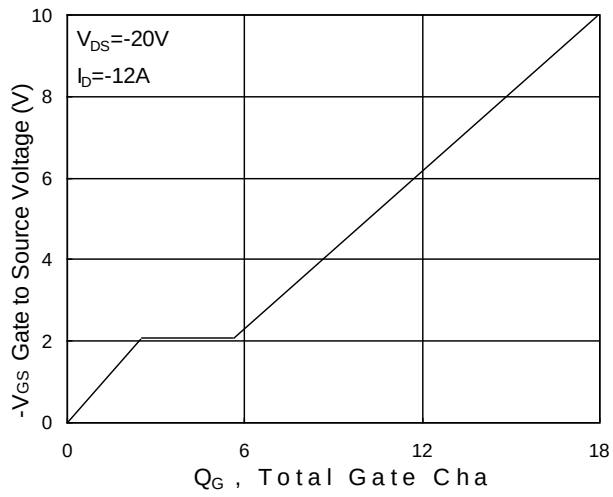


Fig.4 Gate-Charge Characteristics

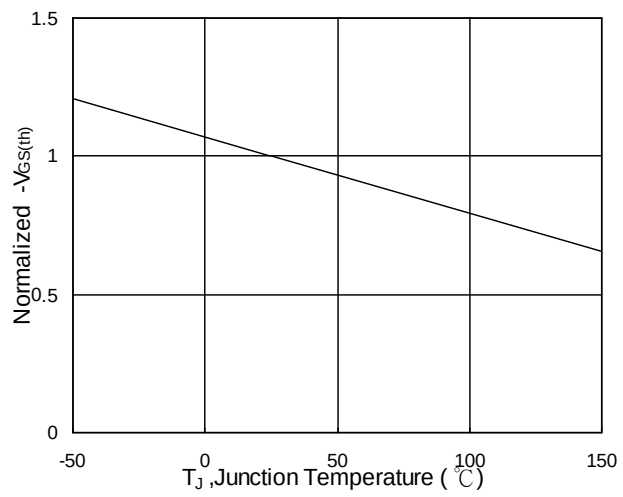


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

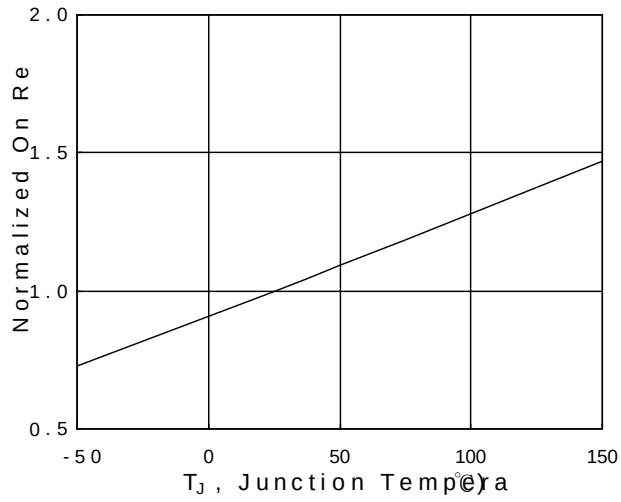
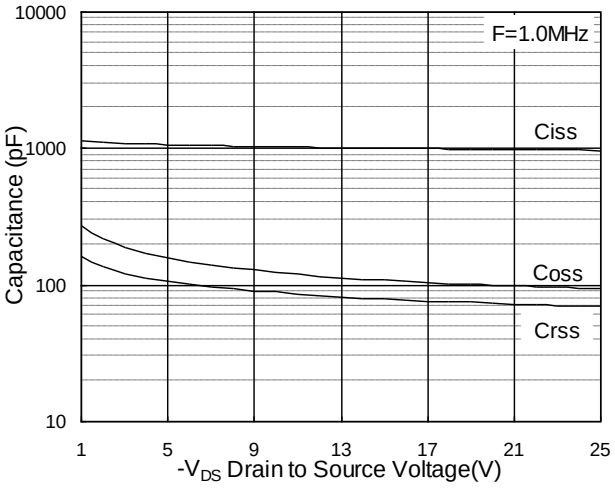


Fig.6 Normalized R_{DSON} v.s T_J

● P-Channel Typical Characteristics(cont.)



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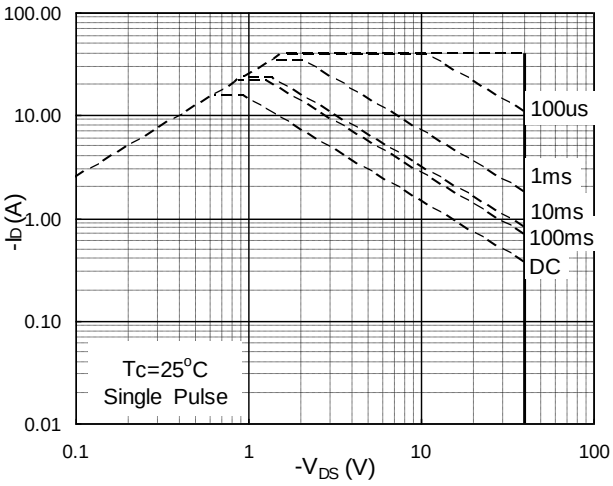

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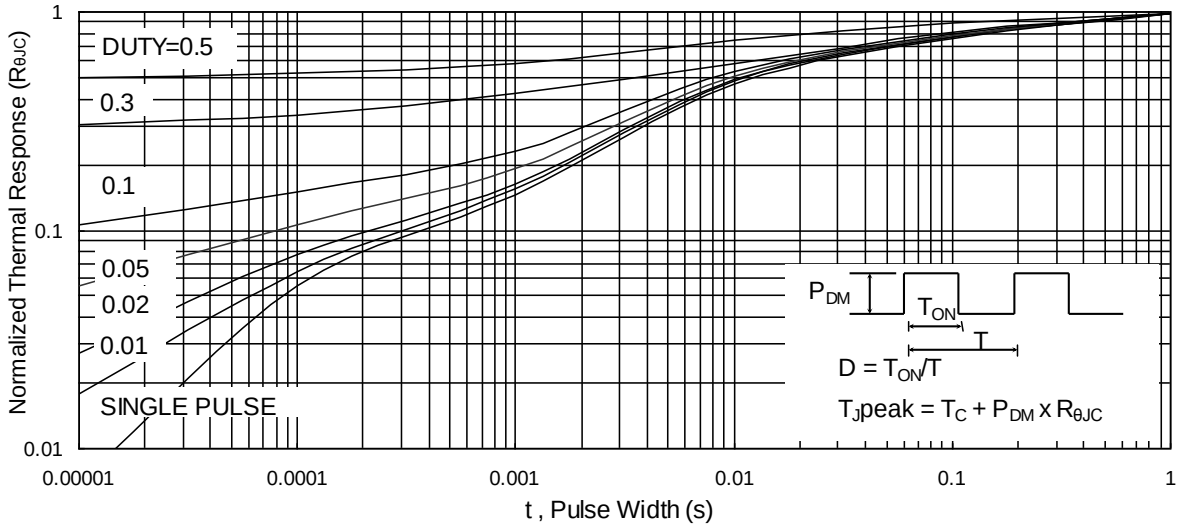

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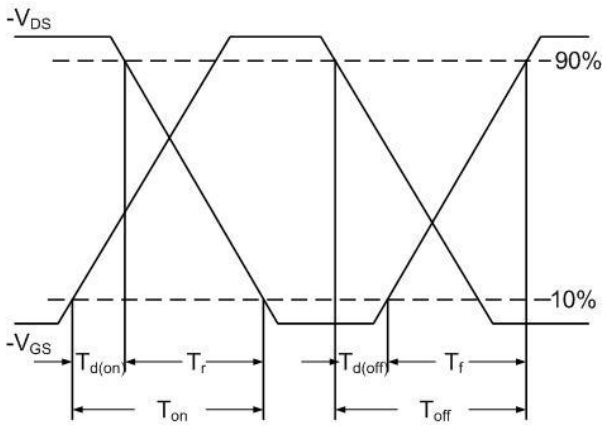

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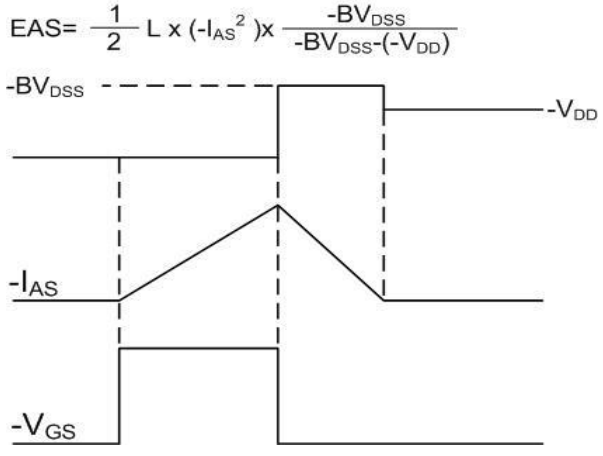

Fig.11 Unclamped Inductive Waveform